This listing of claims will replace all prior versions, and listings, of claims in the application:

IN THE CLAIMS:

Claims 1-9 (cancelled)

Claim 10 (Original): A method of fabricating a recessed channel CMOS device comprising the step of:

providing a patterned oxide layer over an SOI layer, said patterned oxide layer exposing a portion of said SOI layer;

thinning the exposed portion of the SOI layer to form a recessed channel region;

forming a gate dielectric on said recessed channel region;

forming sacrificial nitride spacers on portions of said gate dielectric so as to protect exposed walls of said SOI layer and said oxide layer and forming a gate conductor on other portions of the gate dielectric not containing said sacrificial nitride spacers;

recessing the oxide layer exposing SOI layer abutting the recessed channel region;

forming source/drain diffusion regions in said exposed SOI layer abutting the recessed channel region; and

removing the sacrificial nitride spacers and forming extension implant regions in said SOI layer such that said extension implant regions have an abrupt lateral profile and are located beneath the gate conductor.

Claim 11 (Original): The method of Claim 10 wherein said thinning is carried out by chemical downstream etching, reactive-ion etching, or thermal oxidation and etching.

Claim 12 (Original): The method of Claim 10 wherein said thinning is carried out by thermal oxidation and a chemical oxide removal (COR) process.

Claim 13 (Original): The method of Claim 12 wherein said COR process is carried out at relatively low pressures of 6 millitorr or less and in a vapor of HF and NH_3.

Claim 14 (Original): The method of Claim 10 wherein said source/drain diffusion regions are formed by ion implantation and annealing.

Claim 15 (Original): The method of Claim 10 wherein said source/drain extension and halo implant regions are formed by angled implantation and annealing.

Claim 16 (Original): The method of Claim 10 further comprising forming permanent spacers on exposed sidewalls of said gate conductor and said gate dielectric.

Claim 17 (Original): The method of Claim 10 wherein said gate conductor is a polysilicon gate conductor that is formed by deposition and ion implantation.

Claim 18 (Original): The method of Claim 10 further comprising forming trench isolation regions in said SOI layer.

Claim 19 (Original): The method of Claim 10 further comprising forming halo implant regions after forming said extension implant regions, said halo implant regions having an abrupt lateral profile which are located beneath said gate conductor.

Claim 20 (Original): The method of Claim 19 wherein said halo implant regions are formed by angled implantation and annealing.